What is claimed is:

1. A method of designing a semiconductor integrated circuit, comprising the following steps:

a first step for determining the number of clocks different in delay amount, which are used for verification of a circuit design of the semiconductor integrated circuit upon the circuit design thereof and determining delays in the clocks on the basis of pre-set conditions for constraints of timings;

a second step for allocating clocks supplied to respective circuits; and

a third step for optimizing the timings on the basis of a list obtained by the timing constraint conditions and the clock allocation and determining whether results of analyses of the respective timings correspond to violation of the constraints,

wherein the optimization of the timings is repeated according to the constraint violation.

2. A method according to claim 1, further comprising the steps:

a fourth step for generating the clocks different in the delay amount for the verification of a layout design of the semiconductor integrated circuit upon the layout design thereof;

a fifth step for adjusting skews every said

different clocks;

a sixth step for adjusting delays respectively included in the clocks to the determined clock delays upon the layout design, respectively; and

a seventh step for making an adjustment to a layout that satisfies the timing constraint conditions upon the layout design and determining whether analytical results of the respective timings correspond to the constraint violation,

wherein the layout adjustment is repeated according to the constraint violation.

3. A method according to claim 1, further comprising an eighth step for adjusting the value of each of the clock delays again according to the constraint violation when the constraint violation exists in the third step.

4. A method according to claim 1, further comprising a ninth step for adjusting delays set every said clocks according to the constraint violation when the constraint violation occurs in the seventh step.

5. A method according to claim 1, which adds a delay taken up to the output of data at a starting point where the data is outputted, a time interval required to set up the data, a delay developed with a path between

respective circuits and a delay in the clock to be used, and determines the allocated clock delays according to the difference between the added value and the cycle of the clock.